AMENDMENTS TO THE SPECIFICATION

I. Please replace the paragraph beginning on page 1, line 21, and ending on page 2, line 2, with the following amended paragraph:

In particular, LCD panels are changed from super twist nematic (STN) to thin film transistor (TFT) and an organic electroluminescent (EL) display capable of performing a signal response faster than a TFT LCD is under development. Also, a portable terminal adopts functions of processing various kinds of sounds such as a 40-chord bell sound function and various kinds of images taken by a 300,000-pixel digital camera. In contrast, the size of the portable terminal becomes more compact. Thus, the portable terminal confronts a double difficulty that should embody a high-speed signal processing within a limited space.

II. Please replace the paragraph on page 12, lines 5 - 9, with the following amended paragraph:

FIG. 4 shows a more extended range selectable address decoder 30 according to a second embodiment of the present invention, in which four bits are input as values of high and low addresses, respectively. Similarly to the first

embodiment, the 4-to-16 range selectable address decoder 30 includes first and second decoders 31 and 32 formed of a 4-to-16 decoder, respectively, and first through thirtieth XOR gates 33 (XOR1, XOR2, ... , XOR29, and XOR30) for outputting output addresses A0, A1, ... , A14, and A15.

III. Please replace the six consecutive paragraphs beginning on page 19, line 7, and ending on page 20, line 12, with the following amended paragraphs:

First, as shown in FIG. 9A, a low enable signal LOW-EN for selecting and enabling a low group (low) is obtained as $0000\_0000\_0000\_1000_2$ which is output from the low enable signal generator 45 which logically ANDs $0000\_0000\_0011\_1100_2$ (Shift Right) which is obtained by shifting the output of the first range selectable decoder 42 by one bit to the right in the right shift register 51 (SR-R), the output $0000\_0000\_0111\_1000_2$ of the first range selectable decoder 42, and $1111\_1111\_0000\_1111_2$ (~Shift Left) which is obtained by shifting the output of the first range selectable decoder 42 by one bit to the left in the left shift register 52 (SR-L) and then inverting the shifted result in a first inverter 53.

The value of $0000\_0000\_0000\_1000_2$ (LOW-EN) which is output from the

low enable signal generator 45 means enabling of the fourth group.

Similarly to the above low group, as shown in FIG. 9B, a middle enable signal MID-EN for selecting and enabling a middle group (mid) is obtained as $0000\_0000\_0011\_0000_2$ which is output from the middle enable signal generator 46 which logically ANDs the output $0000\_0000\_0111\_1000_2$ of the first range selectable decoder 42, $0000\_0000\_0011\_1100_2$ (Shift Right) which is obtained by shifting the output of the first range selectable decoder 42 by one bit to the right in the right shift register 51, and $0000\_0000\_1111\_0000_2$ (~Shift Left) which is obtained by shifting the output of the first range selectable decoder 42 by one bit to the left in the left shift register 52.

The value of $0000\_0000\_0011\_0000_2$ (MIN-EN) which is output from the middle enable signal generator 46 means enabling of the fifth and sixth groups.

Also, similarly to the above low and middle groups, as shown in FIG. 9C, a high enable signal HI-EN for selecting and enabling a high group (hi) is obtained as $0000\_0000\_0100\_0000_2$ which is output from the high enable signal generator 47 which logically ANDs the output $0000\_0000\_0111\_1000_2$ of the first range selectable decoder 42, $1111\_1111\_1100\_0011_2$ (Shift Right) which is obtained by shifting the output of the first range selectable decoder 42 by one bit to the right in the right shift register 51, and then inverting the shifted result in a second inverter 54, and 0000_0000_1111_0000 (~Shift Left) which is obtained by shifting the output of the first range selectable decoder 42 by one bit to the left in

the left shift register 52.

The value of $0000\_0000\_0100\_0000_2$ (HI-EN) which is output from the high enable signal generator 47 means enabling of the seventh group.

IV. Please replace the paragraph on page 22, lines 6 - 8, with the following amended paragraph:

An example of graphics which can be realized by using the frame memory device according to a first embodiment of the present invention will be described below with reference to FIGs. 11A through 11C. In Figs.11A through 11C, reference characters A0, A1, ... , A7 designate column and row addresses in the frame memory device.

V. Please replace the paragraph on page 24, lines 3 - 4, with the following amended paragraph:

FIG. 12 is a configurational view schematically showing a frame memory device according to a second embodiment of the present invention. In Fig.12,

reference characters A0, A1, ... , A7 designate column and row addresses in the frame memory device.

VI. Please replace the two consecutive paragraphs on page 24, lines 15 - 23, with the following amended paragraphs:

The general purpose address decoder 70 includes: first and second general purpose 8-to-256 decoders 71 and 72 enabling one output among 256 outputs when 8-bit high and low addresses are input thereto; and 256 OR gates 73 (OR1, OR2, ... , OR256) for logically summing the outputs of an identical level from the first and second 8-to-256 decoders 71 and 72.

Thus, since the general purpose address decoder 70 generates a decoder output enabling one output among 256 outputs when 8-bit high and low addresses are input to the first and second 8-to-256 decoders 71 and 72, and the outputs of the first and second 8-to-256 decoders 71 and 72 are logically summed in the 256 OR gates 73 (OR1, OR2, ... , OR256), the outputs of the two decoders 71 and 72 are generated as row addresses.

VII. Please replace the paragraph on page 25, lines 5 - 9, with the following amended paragraph:

FIG. 13 is a configurational view schematically showing a frame memory device according to a third embodiment of the present invention. In Fig.13, reference characters A0, A1, ... , A7 designate column and row addresses in the frame memory device. The third embodiment is similar to the second embodiment. In the third embodiment, a range selectable address decoder is used as a row address decoder. That is, a general purpose address decoder shown in FIG. 15 is used as a column address decoder structure.

VIII. Please replace the paragraph on page 25, lines 17 - 20, with the following amended paragraph:

FIG. 14 is a configurational view schematically showing a frame memory device according to a fourth embodiment of the present invention. In Fig.14, reference characters A0, A1, ... , A7 designate column and row addresses in the frame memory device. In the frame memory device according to the fourth embodiment of the present invention, a general purpose decoder shown in FIG. 15 is used as column and row address decoders 70a and 70.